CLAIMS

What is Claimed is:

1. A method of fabricating a floating gate for a semiconductor device, said method comprising:

depositing an undoped polycrystalline silicon layer on a tunnel oxide layer, wherein said undoped polycrystalline silicon layer has a first thickness; and

depositing a doped polycrystalline silicon layer on said undoped polycrystalline silicon layer, wherein said doped polycrystalline silicon layer has a second thickness, and wherein said undoped polycrystalline silicon layer and said doped polycrystalline silicon layer form said floating gate having a third thickness.

2. The method as recited in Claim 1 wherein said doped polycrystalline silicon layer includes an N-type dopant material.

3. The method as recited in Claim 2 wherein N-type dopant material is phosphorous.

4. The method as recited in Claim 1 further comprising:

performing a plurality of thermal processes.

5. The method as recited in Claim 1 wherein said third thickness is approximately a sum of said first thickness and said second thickness.

6. The method as recited in Claim 1 wherein said first thickness is approximately one third of said third thickness, and wherein said second thickness is approximately two thirds of said third thickness.

7. The method as recited in Claim 1 wherein said first thickness is approximately fifty percent of said third thickness, and wherein said second thickness is approximately fifty percent of said third thickness.

8. The method as recited in Claim 1 wherein said semiconductor device is a flash memory device.

9. A method of fabricating a stacked gate structure for a semiconductor device, said method comprising:

forming a tunnel oxide layer on a surface of a semiconductor substrate;

depositing an undoped polycrystalline silicon layer on said tunnel oxide layer, wherein said undoped polycrystalline silicon layer has a first thickness;

depositing a doped polycrystalline silicon layer on said undoped polycrystalline silicon layer, wherein said doped polycrystalline silicon layer has a second thickness, and wherein said undoped polycrystalline silicon layer and said doped polycrystalline silicon layer form a floating gate having a third thickness;

forming a ONO (Oxide-Nitride-Oxide) layer on said floating gate; and

forming a control gate on said ONO layer.

10. The method as recited in Claim 9 wherein said doped polycrystalline silicon layer includes an N-type dopant material.

11. The method as recited in Claim 10 wherein N-type dopant material is phosphorous.

12. The method as recited in Claim 9 further comprising:

performing a plurality of thermal processes.

13. The method as recited in Claim 9 wherein said third thickness is approximately a sum of said first thickness and said second thickness.

14. The method as recited in Claim 9 wherein said first thickness is approximately one third of said third thickness, and wherein said second thickness is approximately two thirds of said third thickness.

15. The method as recited in Claim 9 wherein said first thickness is approximately fifty percent of said third thickness, and wherein said second thickness is approximately fifty percent of said third thickness.

16. The method as recited in Claim 9 wherein said semiconductor device is a flash memory device.

17. A semiconductor device comprising:

a tunnel oxide layer; and

a floating gate formed by depositing an undoped polycrystalline silicon layer on said tunnel oxide layer and depositing a doped polycrystalline silicon layer on said undoped polycrystalline silicon layer, wherein said undoped polycrystalline silicon layer has a first thickness, wherein said doped polycrystalline silicon layer has a second thickness, and wherein said floating gate has a third thickness.

18. The semiconductor device as recited in Claim 17 wherein said doped polycrystalline silicon layer includes an N-type dopant material.

19. The semiconductor device as recited in Claim 18 wherein N-type dopant material is phosphorous.

20. The semiconductor device as recited in Claim 17 wherein said third thickness is approximately a sum of said first thickness and said second thickness.

21. The semiconductor device as recited in Claim 17 wherein said first thickness is approximately one third of said third thickness, and wherein said second thickness is approximately two thirds of said third thickness.

22. The semiconductor device as recited in Claim 17 wherein said first thickness is approximately fifty percent of said third thickness, and wherein said second thickness is approximately fifty percent of said third thickness.

23. The semiconductor device as recited in Claim 17 wherein said semiconductor device is a flash memory device.